Optimizing PCB Thermal Performance for Cree® XLamp® LEDs

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Application Note: CLD-AP37 Rev. 0

1. Introduction

This design note outlines a technique to assist with the development of cost effective thermal management for the XP and MX families of XLamp LEDs.

One of the most critical design parameters in LED illumination system is the system's ability to draw heat away from the LED junction. High operating temperatures at the LED junction adversely affect the performance of LEDs, resulting in decreased light output and lifetime [1]. In order to properly manage this heat, specific practices should be followed in the design, assembly and operation of LEDs in lighting applications.

This application note outlines a technique for designing a low-cost printed circuit board (PCB) layout which optimizes the transfer of heat from the LED. The technique involves the use of FR-4-based PCBs, which cost less, but have greater thermal resistance than metal core printed circuit boards (MCPCB). The use of metal-lined holes or vias underneath LED thermal pads is a method to dissipate heat through an FR-4-PCB and into an appropriate heat sink.

Using metalized vias is a technique available to the LED packaging used by Cree XLamp LEDs. Electrically isolated thermal pads are a requirement for using this technique. For certain illumination systems design, thermal vias enable the use of FR-4 circuit boards over metal core circuit boards. This can deliver system cost savings in circuit board and heat sink selection.

This application note serves as a practical guideline based on heat transfer fundamentals and includes suggestive, but not definitive, simulation and measurement data. Cree advocates this technique as appropriate design for certain lighting applications and encourages Cree's customers to evaluate this option in considering the many thermal management techniques available. For additional guidelines on LED thermal management refer to application note, Cree XLamp LED Thermal Management.

2. Thermal Management Principles

2.1 XLamp Thermal Characteristics

All XLamp LED packages have an electrically isolated thermal pad. The pad provides an effective channel for heat transfer and optimizes thermal resistance from the LED chip junction to the thermal pad. The pad is electrically isolated from either the anode or cathode of the LED and can be soldered or attached directly to grounded elements on the board or heat sink system.

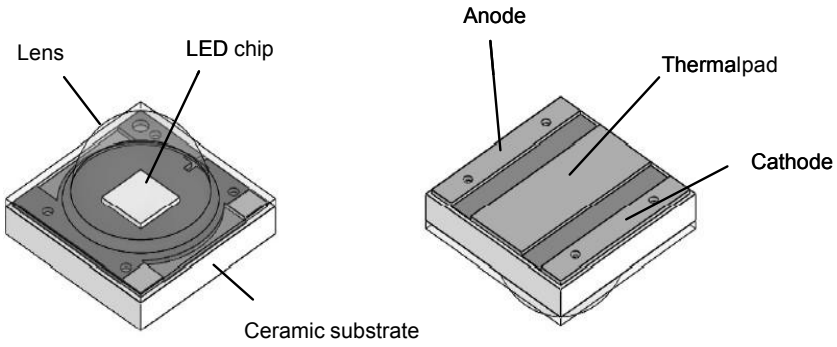

Figure 1. Cree XLamp LED package

1 See "Cree® XLamp® Long-Term Lumen Maintenance," CLD-AP28 - http://www.cree.com/products/pdf/XLampXR-E_lumen_maintenance.pdf

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Heat is conducted from LED package through the thermal pad and into a PCB which should be mounted to a heat sink so as to transfer the conducted heat into the operating environment [2].

The following table lists typical thermal resistance values (junction to solder point) for various XLamp series LEDs.

Color	XP-C	XP-E	XP-G	MX-6
White (cool, neutral, warm)	12 ºC/W	9 ºC/W	6 ºC/W	5 ºC/W
Blue	12 ºC/W	9 ºC/W	---	---
Green	20 ºC/W	15 ºC/W	---	---
Amber, red, red-orange	15 ºC/W	10 ºC/W	---	---

Table 1. Typical thermal resistance (ºC/W) values for Cree XLamp LEDs

2.2 PCB thermal characteristics

FR-4

FR-4 is one of the most commonly used PCB materials and is the NEMA designation for a flame retardant, fiber-glass reinforced epoxy laminate. A bi-product of this construction is that FR-4 has very low thermal conductivity. Figure 2 below shows a typical cross-sectional geometry for a two-layer FR-4 board.

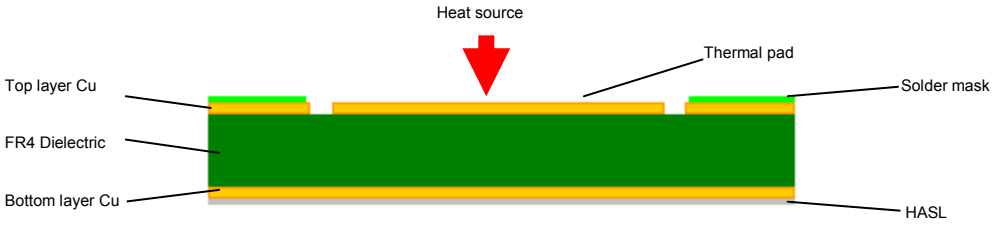

Figure 2. FR-4 cross-sectional geometry (not to scale)

Using the thermal conductivity values in table 2 below, the total thermal resistance for an FR-4 board can be characterized by adding up the thermal resistances for each of the layers.

$$\theta_{PCB} = \theta_{layer1} + \theta_{layer2} + \theta_{layer3} \ldots + \theta_{layerN} \quad (1)$$

For a given layer the thermal resistance is given by the formula:

$$\theta = l / (k \times A) \quad (2)$$

where l is the layer thickness, k is the thermal conductivity, and A is the area normal to the heat source. For a 1.6-mm-thick star board with an area of approximately 270 mm [2], the through-plane thermal resistance is approximately 30 ºC/W [3].

2 For this document and subsequent discussion and simulation, we assume a theoretically infinite heat sink which maintains the back side of the board to 25ºC.

3 Bear in mind that this calculation is only one-dimensional and does not account for the size of the heat source and spreading, convection thermal resistances or boundary conditions.

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Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
FR-4	1588	0.2
Bottom layer copper	70	398
ENIG (Electroless Nickel/Immersion Gold)	35	58

Table 2. Thermal conductivities of FR-4 board layers

Metal-Core Printed Circuit Board

A simple one layer MCPCB has 4 layers: the solder mask, copper circuit layer, thermally conductive dielectric layer, and metal core base layer as shown below in Figure 3. These three layers are then laminated and bonded together providing a path for the heat to dissipate. Often the metal substrate is aluminum, though steel and copper can also be used.

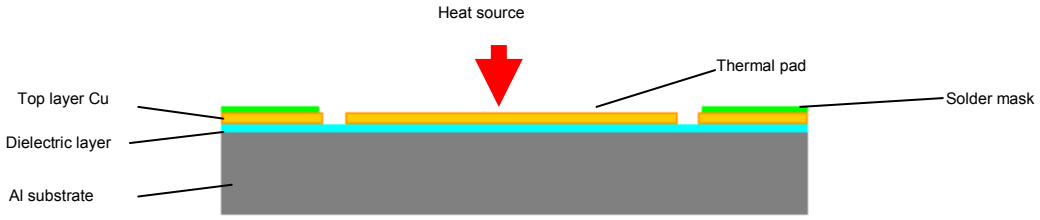

Figure 3. MCPCB cross-sectional geometry (not to scale)

Using the thermal conductivity values in table 3 below, the one-dimensional through-plane thermal resistance for the same-sized board is roughly 0.2 ºC/W.

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
PCB dielectric	100	2.2
Al plate	1588	150

Table 3. Thermal conductivities of MCPCB layers

2.3 Designing Thermal Vias

An inexpensive way to improve thermal transfer for FR-4 PCBs is to add thermal vias - plated through-holes (PTH) between conductive layers. Vias are created by drilling holes and copper plating them, the same way that a PTH or via is used for electrical interconnections between layers.

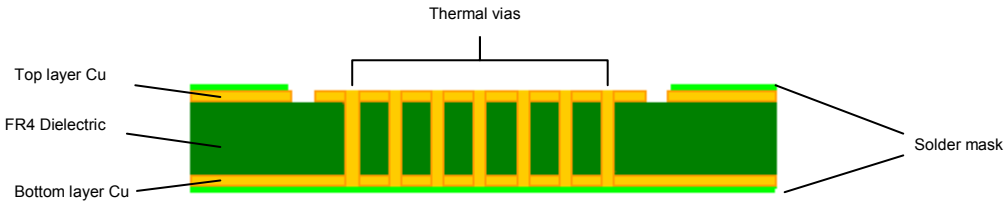

Figure 4. FR-4 geometry with thermal vias (not to scale)

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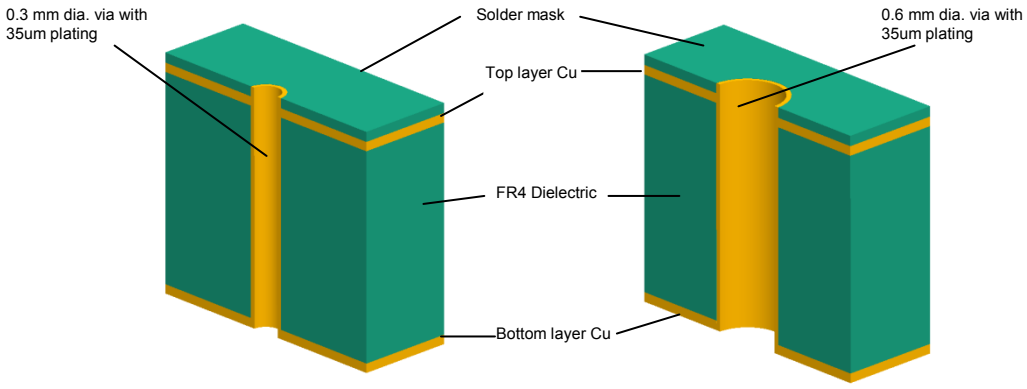

Figure 5. Cross-sectional geometry of small and large thermal vias in FR-4 substrate

Adding vias in an appropriate way will improve the thermal resistance of an FR-4 board. The thermal resistance of a single via can be calculated by the same formula, $\theta = l / (k \times A)$. Using the values in Table 4, a single solid via with a diameter of 0.6 mm results in $(1.588 \times 10^{-3}) / (58 \times (\pi \times (0.5 \times 0.6 \times 10^{-3})^2)) = 96.8$ ºC/W. However, when N vias are used, the area increases by a factor of Nvias, resulting in:

$$\theta_{vias} = l / (N_{vias} \times k \times A) \qquad (3)$$

Keep in mind this is applicable only if the heat source is directly normal to the thermal via; otherwise, the resistance will increase due to thermal spreading effects. To calculate the total thermal resistance for the region underneath (or normal to) the LED thermal pad, the equivalent thermal resistance for the dielectric layer and vias should be determined. For simplicity, the two resistances are treated as parallel applying this formula:

$$\theta_{vias \;||\; FR\text{-}4} = [\; (1/\theta_{vias}) + (1/\theta_{FR\text{-}4}) \;]^{-1} \qquad (4)$$

Using the values in table 4, for a 270mm2 board with five 0.6mm diameter solid vias results in an approximate thermal resistance of 12ºC/W, a 250% improvement over the initial 30ºC/W derived in from the data in Table 2.

Layer/Material	Thickness (µm)	Thermal conductivity (W/mK)
SnAgCu solder	75	58
Top layer copper	70	398
FR-4	1588	0.2
Filled vias (SnAgCu)	1588	58
Bottom layer copper	70	398
Solder mask (optional)	25	0.2

Table 4. Thermal conductivities of FR-4 board layers including thermal vias

2.4 Open Vias vs. Filled Vias

Open vias will result in a higher thermal resistance compared to filled vias because the area normal to the heat source is reduced per the formula:

$$A = \pi \times (D \times t - t^2) \qquad (5)$$

where D is the via diameter and t is the plating thickness.

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For a 0.6-mm diameter via with 35-µm (1 oz.) copper plating, the area (normal to the thermal pad) is only 0.06 mm^2 compared to 0.28 mm^2 for a solid via, resulting in a thermal resistance of 441 ºC/W per via compared to 96.8 ºC/W. For the same sized board and number of vias as in the previous example, the resulting through-plane thermal resistance becomes ~28 ºC/W.

However, the ability to create solid (copper) filled vias delivers additional reduced thermal resistance, as compared to vias filled with SnAgCu solder.

In general, increasing plating thickness during PCB production will improve thermal resistance of vias. Consult with your PCB manufacturer to determine if thicker plating is feasible.

Non-filled vias may become filled with solder during reflow. However, depending on a number of factors, this may not occur reliably. The vias, if not reliably filled, are not an effective heat management tool.

Other than creating a solid via during the plating process in PCB production, another option is to fill the vias with copper (or some other thermally conductive material such as conductive epoxy) as part of the PCB fabrication process. But this adds an additional step to fabrication and may increase the cost of the board.

Solder voiding in open PTH vias

Figure 6a shows an example of unfilled vias after reflow, and Figure 6b shows an example of solder voids underneath the device (shown in red). The voids will increase the thermal resistance of the thermal interface. Also, the solder may overfill the hole leading to bumps on the bottom of the board which can reduce contact area between the board and heat sink. Steps can be taken to limit the amount of solder wicking. One way is to maintain a via diameter smaller than 0.3 mm. With smaller vias, the surface tension of the liquid solder inside the via is more capable of countering the force of gravity on the solder. If the via structure is constructed following the guidelines mentioned above, holding inside via diameter to around 0.25 mm – 0.3 mm, minimal solder wicking is achieved. The drawback to this approach is that smaller open vias will result in a higher overall thermal resistance.

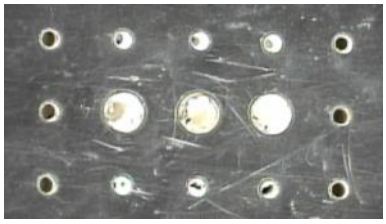

Figure 6a. Unfilled vias

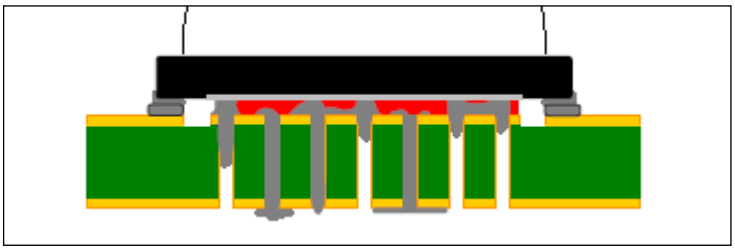

Figure 6b. Solder voiding (not to scale)

Another technique for limiting solder wicking involves using solder mask to restrict the flow of solder from the top side of the PCB to the bottom side. One process, called "tenting," uses solder mask to prevent solder from either entering or exiting the thermal vias, depending on the side of the board to which the solder mask is placed. Tenting the bottom side with solder mask to cover and plug the thermal vias can prevent solder from flowing down into the via and onto the bottom of the board. In top-side via tenting, small areas of solder mask are placed over the thermal vias on the top side of the PCB to prevent solder from flowing into the vias from the top side of the board.

Figure 7: Tented vias with bottom-side solder mask (not to scale)

In general, Cree advocates creating copper-filled vias as being a more practical and effective technique, preferable to solder-filled vias.

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3. Thermal Performance Simulations

The following section presents results obtained from computational thermal analysis for a series of PCB configurations [4].

3.1 Surface Thermal Dissipation

The first configuration, as shown in Figure 8, consists of a star FR-4 PCB with varying widths for the thermal pad and two board thicknesses (0.8 mm and 1.6 mm); the bottom copper layer is solid, and there are no thermal vias.

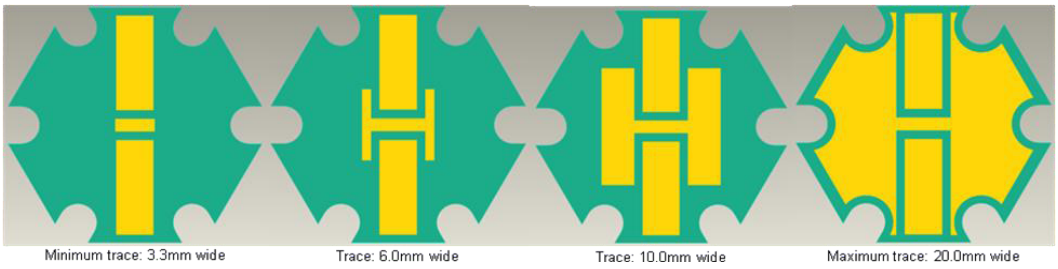

Figure 8: Variation in thermal pad width on top side of PCB

The results shown in Chart 1 show for the 1.6mm-thick board increasing the width beyond 12 mm provides little improvement, while for the 0.8-mm-thick board, the improvement tapers off beyond a width of 16 mm.

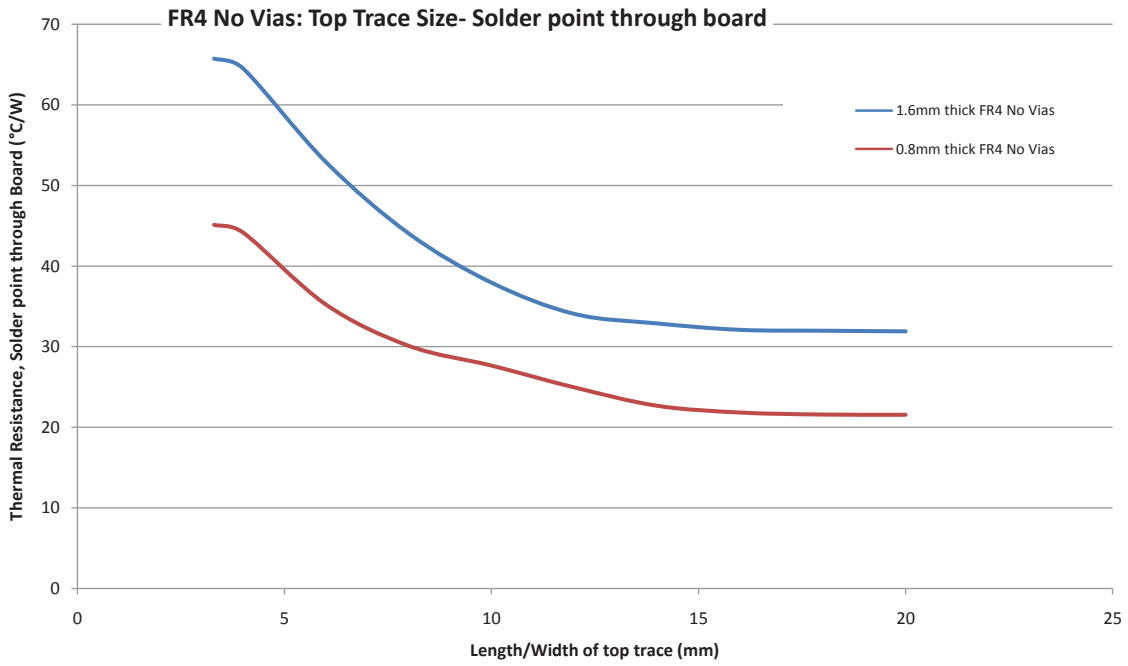

Chart 1: Thermal resistance for FR-4 PCB with no vias with varying thermal pad size

The next configuration is the same except the board is a MCPCB. Data in chart 2 shows for either board thickness there is little benefit to extending the thermal pad width beyond 6 mm.

4 Cree used Ansys Design Space, http://www.ansys.com/products/structural-mechanics/products.asp

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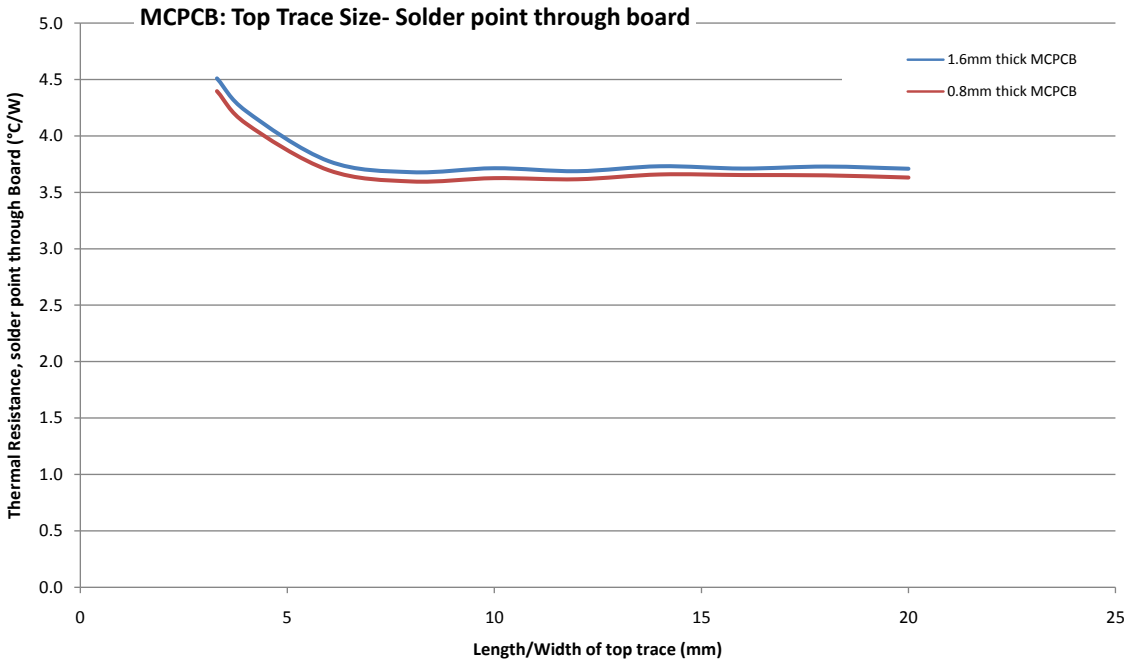

Chart 2: Thermal resistance for MCPCB with varying thermal pad size

3.2 Thermal Dissipation with Vias

Chart 3 shows the effect of various filling materials for 0.7mm-diameter vias with 1mm center-to-center spacing for both 1.6-mm and 0.8-mm board thicknesses as shown in Figure 9. The data indicates solid copper filled vias result in lower thermal resistance while unfilled vias deliver higher thermal resistance. Rounding out the discussion, a via filled with solder or conductive epoxy doesn't perform much better than an unfilled via.

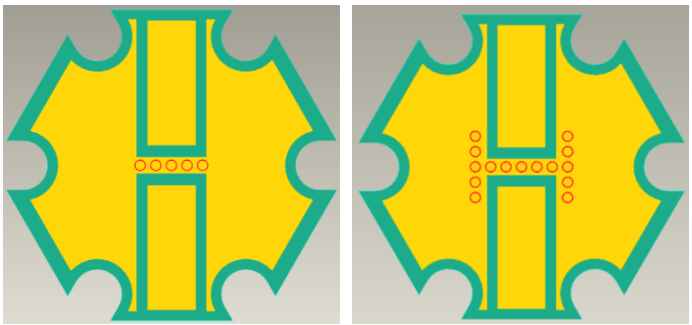

Figure 9: FR-4 board with five and fifteen 0.7-mm-diameter vias and 1-mm pitch

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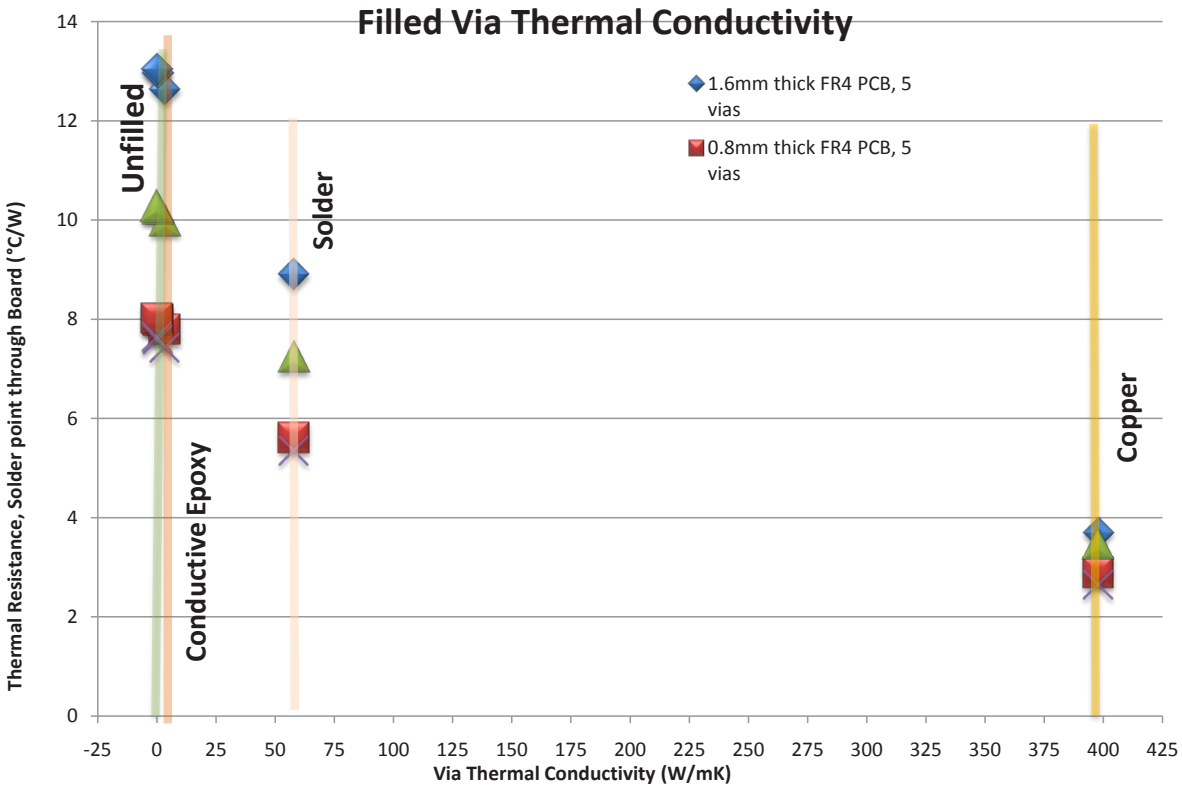

Chart 3: Thermal resistance for FR-4 vias filled with materials of differing conductivity

Chart 4 shows the effect of changing the diameter and number vias. For this chart, the vias are filled with SnAgCu solder. As expected, the larger the diameter of the via, the lower the thermal resistance becomes. Increasing the number of vias shows considerable improvement for smaller via diameters as well.

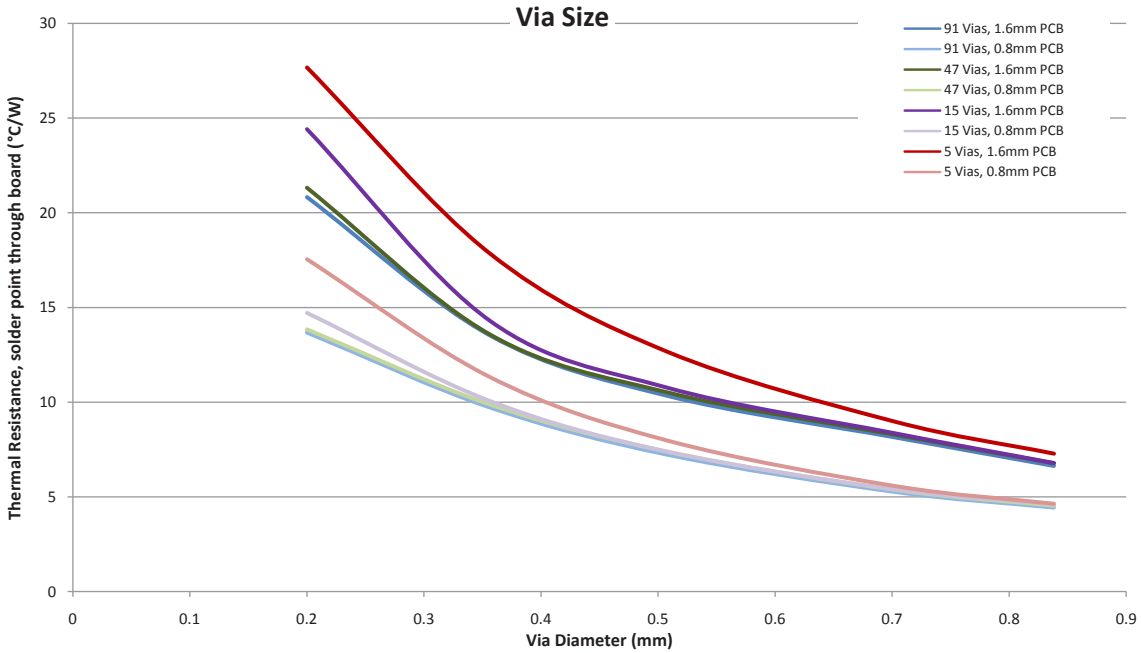

Chart 4: FR-4 PCB with various via diameters and numbers of vias

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The next case considers the effect of varying the number of thermal vias as shown below in Figure 10. These vias are solid plated copper with a diameter of 0.254 mm (0.010”) and center-to-center spacing of 0.635 mm (0.025”). This size was chosen because standard plating techniques can be used to fill the vias without additional processing. The results shown in Chart 5 indicate that increasing the number of vias beyond 14 shows little improvement (this is maximum achievable density of the area normal to the LED thermal pad).

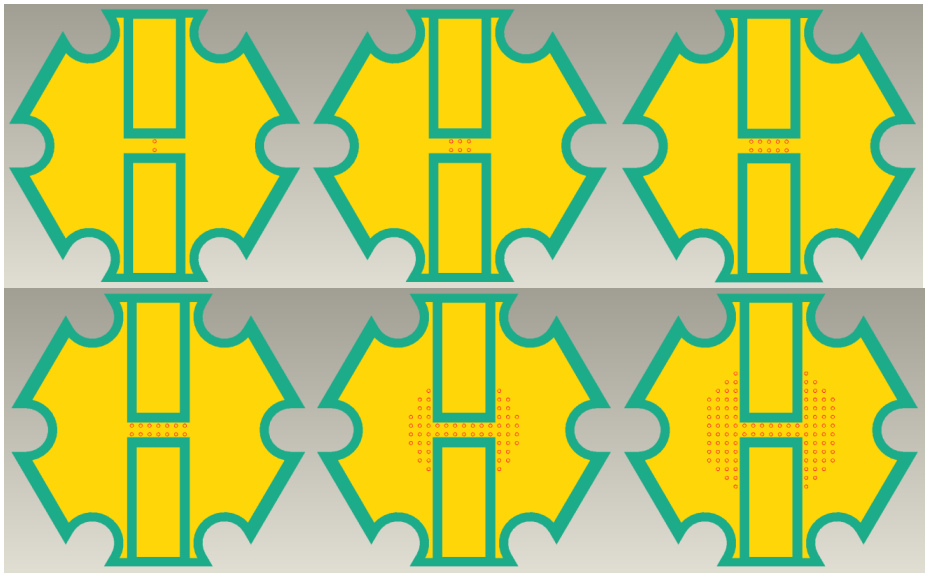

Figure 10: FR-4 board with varying numbers of thermal vias (2, 6, 8, 14, 58, and 102)

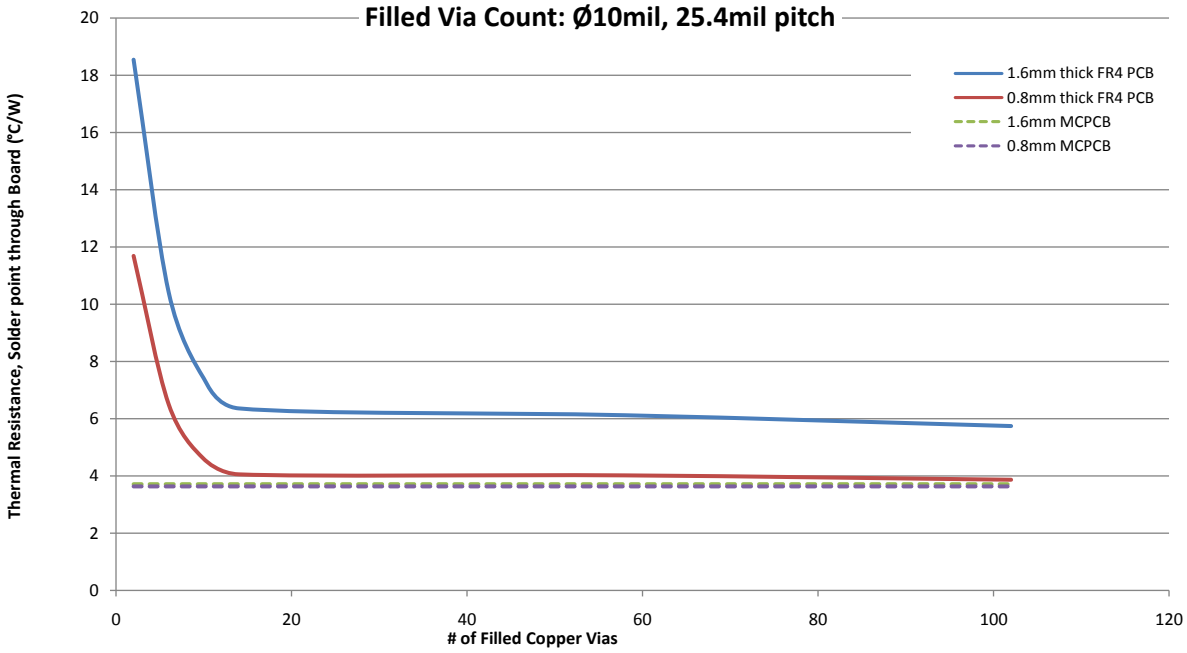

Chart 5: Thermal resistance values FR-4 board for varying numbers of copper-filled thermal vias

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3.3 Combined Surface and Via Studies

The next case that is considered is an FR-4 PCB with 14 0.254mm-diameter solid copper plated vias with varying thermal pad trace widths as shown below in Figure 11. The bottom copper layer is solid. The data in Chart 6 show that beyond a width of 6mm, there is little improvement in thermal resistance.

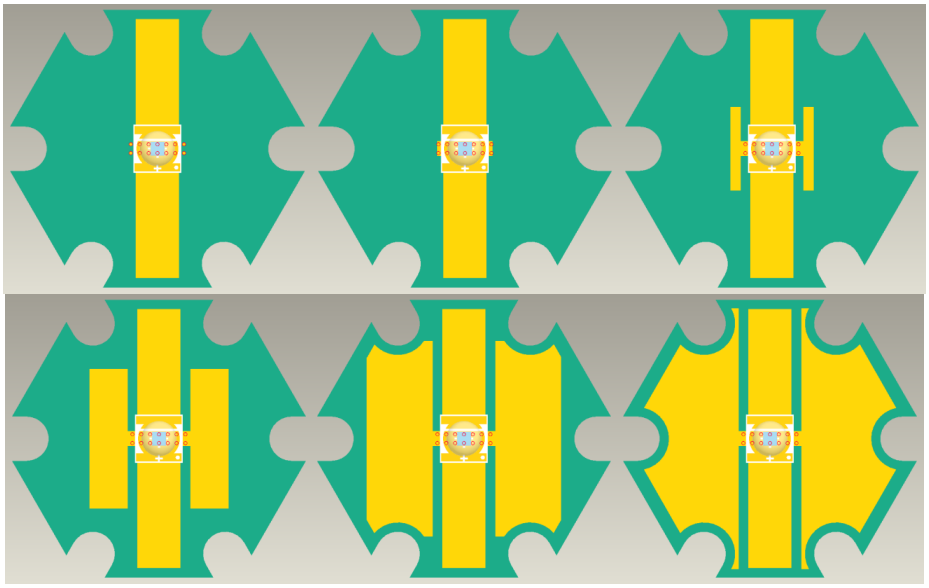

Figure 11: FR-4 PCB with 14 thermal vias and varying top thermal pad widths (3.3, 4.0, 6.0, 10.0, 14.0, 20.0 mm)

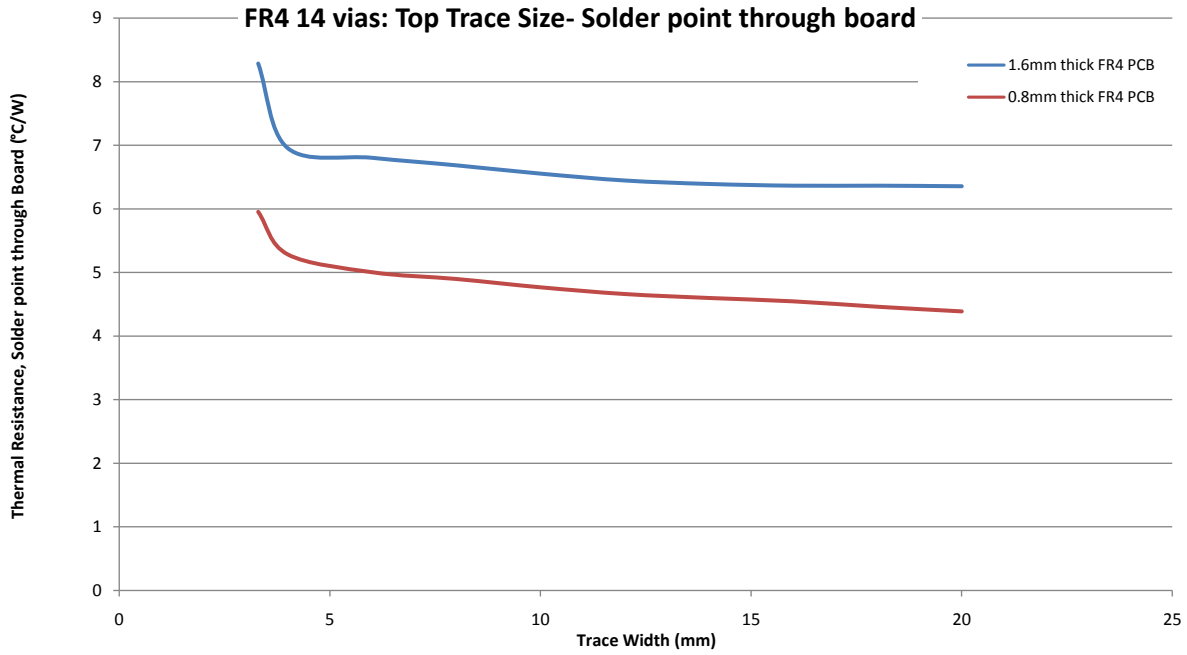

Chart 6: Thermal resistance of FR-4 PCB with 14 vias and varying thermal pad widths

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Finally, the previous scenario is repeated but with various bottom thermal pad trace widths as shown in Figure 12.

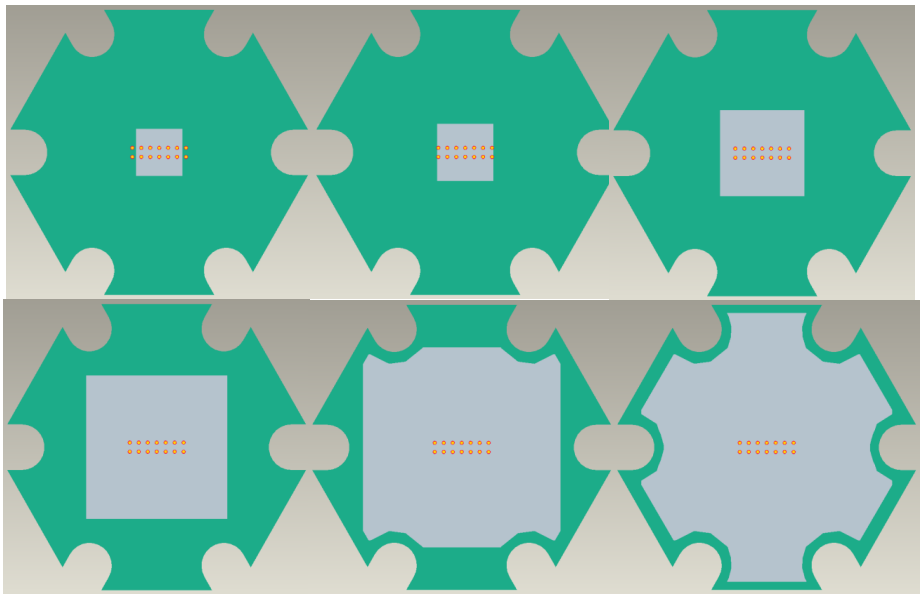

Figure 12: FR-4 PCB with 14 thermal vias and varying bottom thermal pad widths (3.3, 4.0, 6.0, 10.0, 14.0, 20.0 mm)

The results are in Chart 7 and indicate that there is a small difference in thermal resistance which becomes less as the width of the bottom pad is increased.

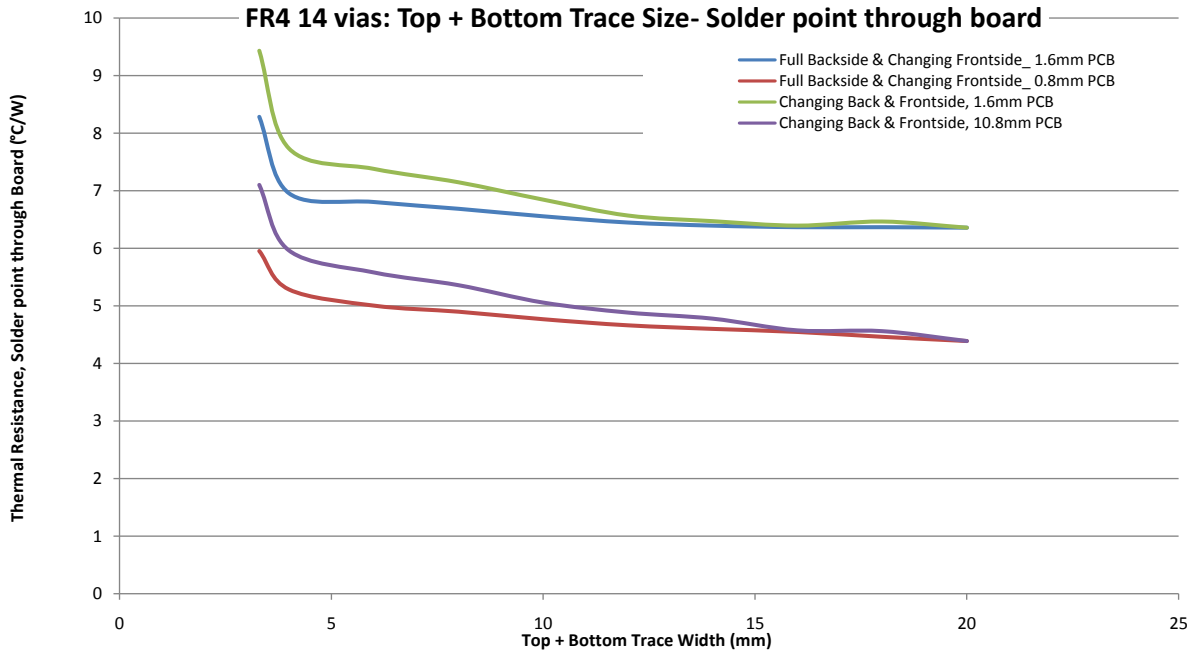

Chart 7: Thermal resistance of FR-4 PCB with 14 vias and varying top and bottom thermal pad widths

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3.4 Summary Results of Thermal Simulations

1. The results from the various simulations show that to achieve the lowest possible thermal resistance for an FR-4 board, the dielectric thickness should be reduced to 0.8mm.
2. While making the vias as large as possible will reduce thermal resistance, the cost of manufacturing the board needs to also be taken into consideration. Larger unfilled vias introduce the possibility of voids or gaps in the materials which might fill the vias. Smaller, solid filled vias are a better solution.
3. Finally, adding additional vias and increasing the width of the thermal pad beyond a certain point have diminishing returns because of thermal spreading resistance.

Based on these conclusions, in section 5 we propose an optimal thermal pad size, via size and spacing that is both thermally effective and manufacturable.

4. Temperature Verification Measurements

Because LED junction temperature will affect LED lifetime, Cree recommends performing a thermal verification test on the LED-board assembly under real-life conditions [5].

In this section we illustrate practical LED board thermal measurement using thermocouples, which also offers some corroboration for the simulations on which we base our recommendations.

Figure 13 shows a type-K thermocouple attached to the top copper layer close to the thermal pad. The solder mask (if present) should be removed to solder the thermocouple to the board. Alternately the thermocouple can also be attached using a thermal epoxy or aluminum tape. If more than one LED is on the board, the Lamp with the highest expected temperature should be selected. Another thermocouple is placed on the front of the heat sink next to the PCB and a third thermocouple is attached to the back of the heat sink. A fourth thermocouple is used to measure the ambient (air) temperature [6]. The thermocouple wires are held in place with Kapton® tape. The temperature measurements for the two heat sink measurements points were recorded after allowing one hour for thermal stabilization. To calculate the actual heat sink-to-ambient thermal resistance, divide the difference between T_{hs} and T_a by the power of the heat source. The calculated value for heat sink in the example was 14.7 ºC/W, which includes the thermal resistance of the attachment method – thermal tape (0.95 ºC/W).

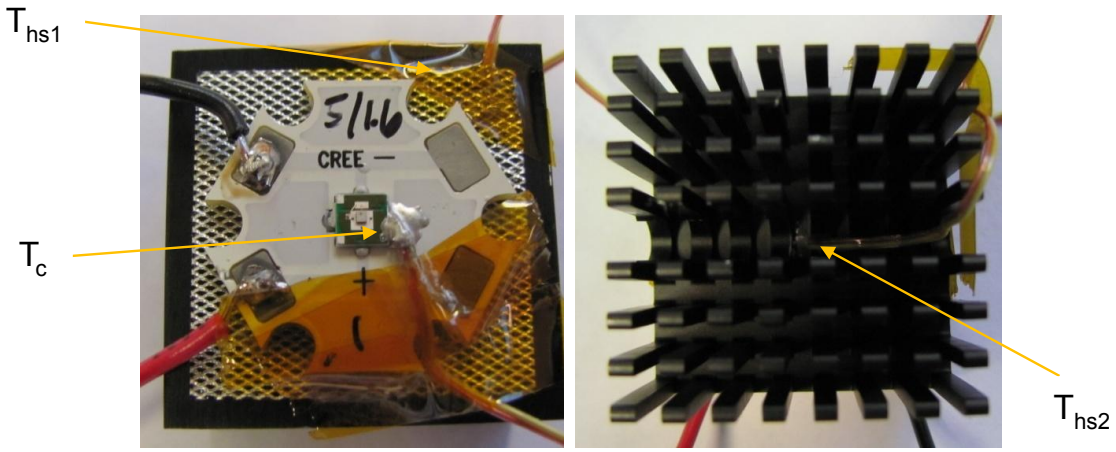

Figure 13: Thermocouple placement

5 However, normally the junction temperature cannot be measured directly and must be derived from the temperature measured at a reference point on the top copper layer.

6 At least 2 mm away from heat sink and/or illumination source and not in the path of illuminance.

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Table 5 below contains data from two sets of XLamp XP-C LEDs mounted on star boards. Three are mounted on 1.6mm-thick FR-4 boards with 5 vias (similar to Figure 9) and three 1.6mm-thick aluminum clad boards. The PCBs were mounted to a heat sink with thermal adhesive [7]. Measurements were taken at 350mA (I_f) and at an ambient temperature of 20 degrees Celsius (T_a) of the forward voltage (V_f), case temperature (T_c). With these measurements the power (P), junction temperature (T_j), case-to- ambient thermal resistance (θ_{ca}), and PCB thermal resistance (θ_{pcb}) can all be calculated per the following equations:

$$P = I_f * V_f \quad (7)$$

$$T_j = T_c + \theta_{jc} \times P \quad (8)$$

$$\theta_{ca} = (T_c - T_a) / P \quad (10)$$

$$\theta_{pcb} = \theta_{ca} - \theta_{hs\text{-}a} \quad (11)$$

1.6-mm FR-4 5 via										
	I_f (mA)	V_f	P (W)	T_c (ºC)	θ_{jc} (ºC/W)	T_j (ºC)	$\theta_{hs\text{-}a}$ (ºC/W)	T_a (ºC)	θ_{ca} (ºC/W)	θ_{pcb} (calc) (ºC/W)
1	350	3.40	1.16	49.4	12	63.6	14.7	20	25.3	10.6
2	350	3.32	1.17	46.6	12	60.6	14.7	20	22.7	8.0
3	350	3.33	1.17	47.2	12	61.2	14.7	20	23.3	8.6
AVG										9.1
1.6-mm MCPCB										
	I_f (mA)	V_f	P (W)	T_c (ºC)	θ_{jc} (ºC/W)	T_j (ºC)	$\theta_{hs\text{-}a}$ (ºC/W)	T_a (ºC)	θ_{ca} (ºC/W)	θ_{pcb} (calc) (ºC/W)
1	350	3.34	1.17	39.3	12	53.3	14.7	20	16.5	1.8
2	350	3.37	1.17	41.7	12	55.7	14.7	20	18.5	3.8
3	350	3.34	1.15	41.4	12	55.2	14.7	20	18.6	3.9
AVG										3.2

Table 5: PCB temperature measurements

The results are close to the predicted performance in Chart 2 (which indicates a thermal resistance asymptote of about 3.5 ºC/W for MCPCB) and Chart4 (which shows a 5-via 1.6mm FR-4 board with a thermal resistance of about 9 ºC/W for a 0.7mm diameter, solder-filled via) [8].

5. Recommended Board Layouts

Simulations confirm expectations – a copper filled via has lower thermal resistance than a solder-filled one. **Cree recommends creating areas of 10-mil (0.254 mm) vias set up on a rectilinear grid of 25 mil (0.635 mm).** The reasons for this choice are for the combination of performance and manufacturability. According to several PCB manufacturers,10-mil holes and 25-mill spacing are reasonable and repeatable production choices and ***when used with a 2-oz. plating solution can be reliably filled with solid copper as part of the board-plating process.*** The simulations in Chart 5 show that 10-mil vias can approach 4 ºC/W on 0.8-mm FR-4 PCBs.

The following sections illustrate minimum recommended pad sizes for the XP and MX packages.

7 Aavid Thermalloy part number 374424B00035G, with Chomerics THERMATTACH® T411 thermal tape.

8 In general, thermal measurement of LEDs is challenging and there is a lot of room for error because of all of the variables involved. Thermocouple placement and subsequent calculations are but two of the concerns. We use these results for their suggestive value rather than their definitive result.

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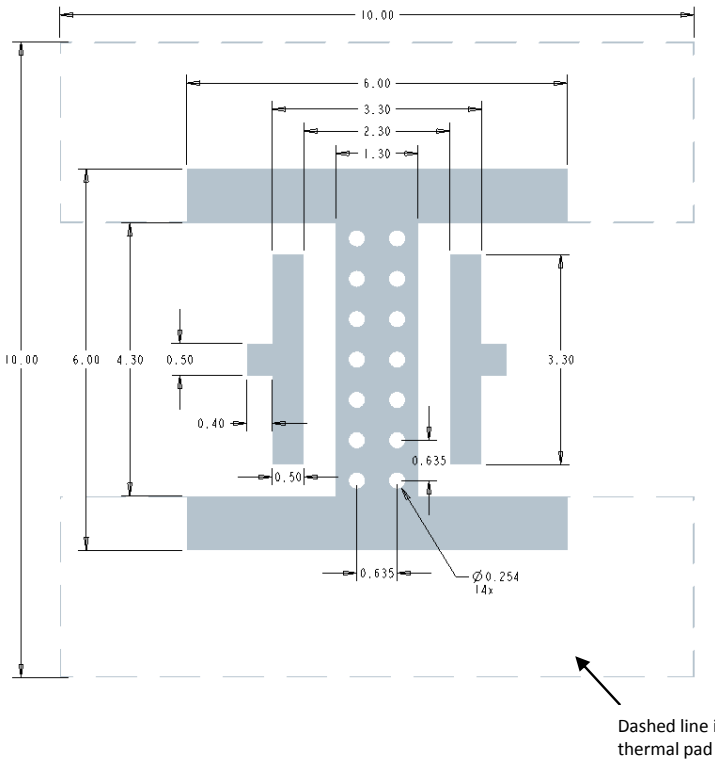
5.1 FR-4 boards for XLamp XP Package

Top



Bottom

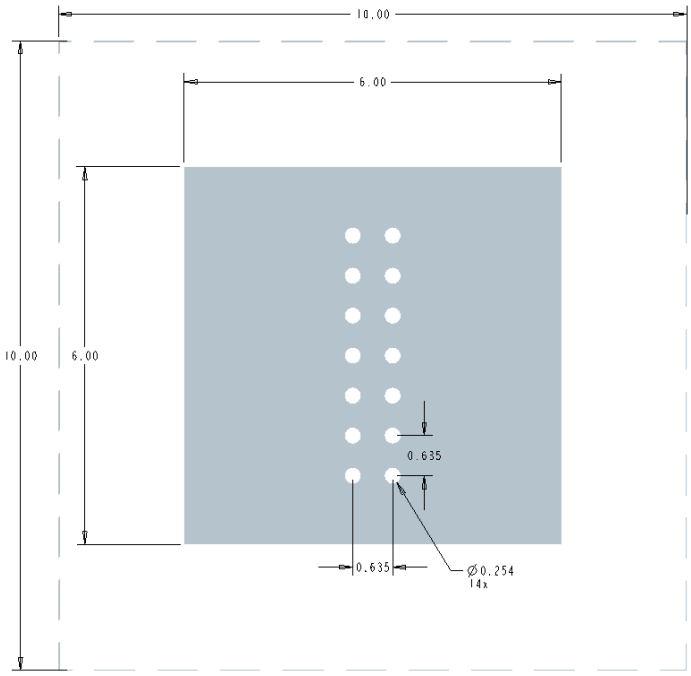


Figure 14: Recommended footprint for XLamp XP family of LEDs on FR-4 PCB (top and bottom)

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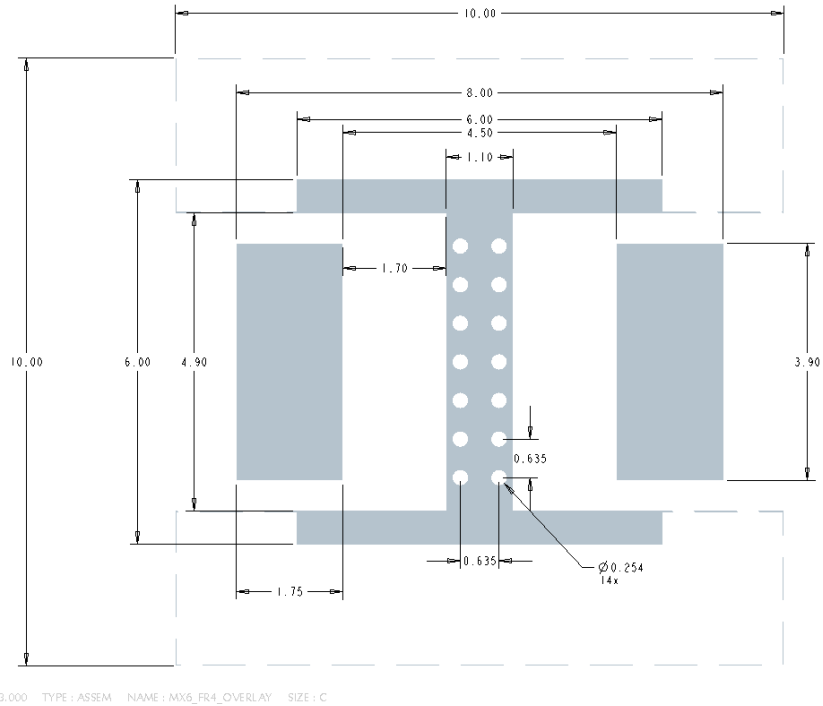
5.2 FR-4 boards for XLamp MX Package

Top



Bottom

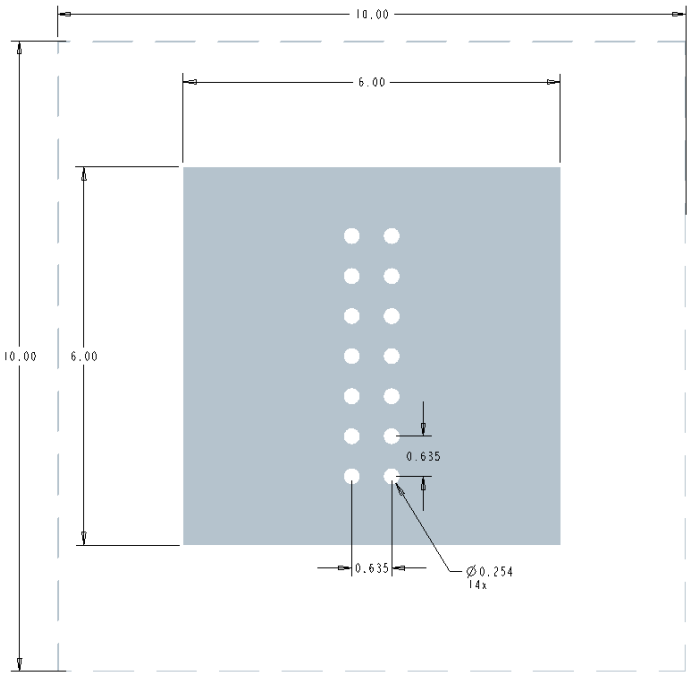


Figure 15: Recommended footprint for XLamp MX package on FR-4 PCB (top and bottom)

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For the MX-6 and XP family of LEDs, Cree has created an updated set of Gerber files for a star-shaped, single LED circuit board. These files are updated to include via drilling specifications. The Gerber files are posted as a .zip archive on the product pages for each of the XP and MX products. When using multiple LEDs, tighter spacing between emitters will result in increased heating. The thermal pads can be connected together and additional copper may be added if possible.

6. Chemical Compatibility

When selecting the interface materials used between the board and the heat sink, as well as other materials to which the LEDs can be exposed, it is important to verify chemical compatibility. Certain materials (e.g., adhesives, solder mask, flux residue) from FR-4 board fabrication and assembly processes can outgas and react adversely with the materials in the LED package, especially at high temperatures, and cause performance degradation and possible product failure. Each family or individual LED product has a corresponding application note. See "Cree® XLamp® LED Soldering & Handling," CLD-AP25[9] for the XLamp XP family and CLD-AP32[10] for the XLamp MX-6 LED, for known substances that are harmful to Cree LEDs[11]. Consult with your PCB manufacturer to determine which specific materials they use.

7. References

Electronics Cooling, September 1997, Vol.3, No.3, "Calculation Corner: One-dimensional heat flow" Bruce M. Guenin, Ph.D., Associate Editor.

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"Thermal and High Current Multilayer Printed Circuit Boards With Thermagon T-lam and Hybrid Boards" January 31, 2001, Thermagon, Inc., Courtney R. Furnival.

"Thermal Considerations for QFN Packaged Integrated Circuits" AN315 rev 1, July 2007, Cirrus Logic, Inc.

9 http://www.cree.com/products/pdf/XLampXP_SolderingandHandling.pdf
10 http://www.cree.com/products/pdf/XLampMX-6_SolderingandHandling.pdf
11 An additional resource is http://outgassing.nasa.gov/

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